In the Claims:

Please amend the claims to read as indicated below.

1. (currently amended) A method of compiling a software program for a programmable processor having a functional unit associated with at least two issue slots, the method comprising:

receiving a set of processor-executable operations comprising a first processor-executable operation of a type typically associated with at least two issue slots and a second processor-executable operation; and

replacing the first processor-executable operation ~~of the type associated with at least two issue slots of the functional unit~~ with a third equivalent processor-executable operation associated with fewer than all of the issue slots, thereby allowing one or more of the rest of the issue slots to be used by the second processor-executable instruction.

2. (currently amended) The method of claim 1, wherein replacing the first processor-executable operation with a third equivalent processor-executable operation further ~~comprising~~ comprises analyzing the first processor-executable operation ~~of the type typically associated with at least two issue slots~~ and external information to determine whether the first processor-executable operation ~~of the type typically associated with at least two issue slots~~ can be replaced by the third equivalent ~~a~~ processor-executable operation ~~associated with fewer than all of the issue slots associated with the functional unit~~.

3. (currently amended) The method of claim 1, wherein ~~replacing the processor-executable instruction comprises replacing the processor-executable operation of the type typically associated with at least two issue slots with an~~ the third equivalent processor-executable operation is associated with only one issue slot.

4. (currently amended) The method of claim 1, wherein ~~replacing the processor-executable instruction comprises replacing the processor-executable operation of the type typically associated with at least two issue slots with an~~ the third equivalent processor-executable operation is associated with a plurality of issue slots.

5. (currently amended) The method of claim 1, wherein replacing the first processor-executable operation with a third equivalent processor-executable operation further ~~comprising~~ comprises:

determining a number of input registers and a number of output registers that are used by the first processor-executable operation ~~of the type typically associated with at least two issue slots~~; and

when the first processor-executable operation ~~of the type typically associated with at least two issue slots~~ uses at most two input registers and one output register, replacing the first processor-executable operation ~~of the type typically associated with at least two issue slots~~ with ~~an~~ the third equivalent processor-executable operation associated with only one issue slot.

6-7. (cancelled)

8. (currently amended) The method of claim 1, wherein the first processor-executable operation ~~of the type typically associated with at least two issue slots~~ is a shuffle operation.

9. (currently amended) The method of claim 1, wherein the first processor-executable operation ~~of the type typically associated with at least two issue slots~~ is a floating point operation.

10. (original) A method of compiling a software program for a programmable processor having a functional unit associated with a plurality of issue slots, the method comprising:

receiving a processor-executable superoperation of a type typically associated with at least two issue slots;

determining a number of input registers and a number of output registers that are used by the superoperation; and

when the superoperation uses at most two input registers and one output register, replacing the superoperation with an equivalent processor-executable operation associated with only one issue slot.

11. (original) The method of claim 10, further comprising:

identifying any source operations that produce a result affecting a result of the superoperation;

placing commands for the source operations in instruction words;

selecting an earliest instruction word from a set of instruction words after the instruction words in which commands for the source operations have already been placed; and

determining whether an instruction word can be constructed that contains any commands already included in the earliest instruction word in addition to a command for the superoperation.

12. (original) The method of claim 11, further comprising:

when an instruction word that contains any commands already included in the earliest instruction word in addition to the command for the superoperation cannot be constructed, selecting a subsequent instruction word; and

determining whether an instruction word that contains any commands already included in the earliest instruction word in addition to the command for the superoperation can be constructed using the subsequent instruction word.

13. (original) The method of claim 10, wherein the superoperation is a shuffle operation.

14. (original) The method of claim 10, wherein the superoperation is a floating point operation.

15. (currently amended) A method of executing ~~an~~ a first instruction that is typically associated with at least two issue slot by a processor having a functional unit associated with a plurality of issue slots, the method comprising:

determining whether the first instruction can be executed using fewer than the at least two ~~all of the~~ issue slots ~~associated with the functional unit~~; and

when the first instruction can be executed using fewer than the at least two ~~all of the~~ issue slots ~~associated with the functional unit~~, ~~mapping~~ replacing the first instruction with a second equivalent instruction associated with ~~to~~ fewer than the at least two ~~all of~~

~~the~~ issue slots thereby allowing one or more of the rest of the issue slots to be used by a third instruction.

16. (cancelled)

17. (currently amended) The method of claim 15, wherein determining whether the first instruction can be executed using fewer than the at least two issue slots further comprises ~~comprising~~:

determining a number of input registers and a number of output registers that are used by the first instruction; and

when the first instruction uses at most two input registers and one output register, replacing ~~mapping~~ the first instruction with the second instruction, the second instruction being associated with ~~to~~ a single issue slot.

18-19. (cancelled)

20. (currently amended) The method of claim 15, wherein the second instruction is associated with ~~further comprising mapping the instruction to~~ two or more ~~a plurality of~~ issue slots.

21. (currently amended) The method of claim 15, wherein the first instruction is a shuffle operation.

22. (currently amended) The method of claim 15, wherein the first instruction is a floating point operation.

23. (currently amended) A processor-readable medium containing processor-executable instructions for:

receiving a set of operations comprising a first operation of a type typically associated with at least two issue slots of a functional unit of a programmable processor and a second operation; and

replacing the first operation of the type typically associated with at least two issue slots by a third equivalent operation associated with fewer than all of the issue slots associated with the functional unit, thereby allowing one or more of the rest of the issue slots to be used by the second operation.

24. (currently amended) The processor-readable medium of claim 23, further containing processor-executable instructions for analyzing the first operation ~~of the type typically associated with at least two issue slots~~ and external information to determine whether the first operation ~~of the type typically associated with at least two issue slots~~ can be replaced by ~~a~~ the third equivalent operation ~~associated with fewer than all of the issue slots associated with the functional unit~~.

25. (currently amended) The processor-readable medium of claim 23, ~~further containing processor-executable instructions for replacing the operation of the type typically associated with at least two issue slots with~~ wherein the third ~~an~~ equivalent operation is associated with only one issue slot.

26. (currently amended) The processor-readable medium of claim 23, further containing processor-executable instructions for:

determining a number of input registers and a number of output registers that are used by the first operation ~~of the type typically associated with at least two issue slots~~; and

when the first operation ~~of the type typically associated with at least two issue slots~~ uses at most two input registers and one output register, replacing the first operation ~~of the type typically associated with at least two issue slots~~ with ~~an~~ the third equivalent operation associated with only one issue slot.

27-28. (cancelled)

29. (currently amended) The processor-readable medium of claim 23, wherein the first operation ~~of the type typically associated with at least two issue slots~~ is a shuffle operation.

30. (currently amended) The processor-readable medium of claim 23, wherein the first operation ~~of the type typically associated with at least two issue slots~~ is a floating point operation.

31. (original) A processor-readable medium containing processor-executable instructions for:

receiving a superoperation of a type typically associated with at least two issue slots of a functional unit of a programmable processor;

determining a number of input registers and a number of output registers that are used by the superoperation; and

when the superoperation uses at most two input registers and one output register, replacing the superoperation with an equivalent operation associated with only one issue slot.

32. (original) The processor-readable medium of claim 31, further containing processor-executable instructions for:

identifying any source operations that produce a result affecting a result of the superoperation;

placing commands for the source operations in instruction words;

selecting an earliest instruction word from a set of instruction words after the instruction words in which commands for the source operations have already been placed; and

determining whether an instruction word can be constructed that contains any commands already included in the earliest instruction word in addition to a command for the superoperation.

33. (original) The processor-readable medium of claim 32, further containing processor-executable instructions for:

when an instruction word that contains any commands already included in the earliest instruction word in addition to the command for the superoperation cannot be constructed, selecting a subsequent instruction word; and

determining whether an instruction word that contains any commands already included in the earliest instruction word in addition to the command for the superoperation can be constructed using the subsequent instruction word.

34. (original) The processor-readable medium of claim 31, wherein the superoperation is a shuffle operation.

35. (original) The processor-readable medium of claim 31, wherein the superoperation is a floating point operation.

36. (currently amended) A processor-readable medium containing processor-executable instructions for:

determining whether a first ~~the~~ instruction that is typically associated with at least two issue slots in a functional unit of a processor can be executed using fewer than the at least two ~~all~~ issue slots ~~associated with a functional unit of a processor~~; and

when the first instruction can be executed using fewer than the at least two ~~all~~ issue slots ~~associated with the functional unit~~, replacing ~~mapping~~ the first instruction with a second equivalent instruction that is associated with ~~to~~ fewer than the at least two ~~all~~ issue slots thereby allowing one or more of the rest of the issue slots to be used by a third instruction.

37. (currently amended) The processor-readable medium of claim 36, further containing processor-executable instructions for analyzing the first instruction and external information to determine whether the first instruction can be executed using fewer than the at least two ~~all~~ issue slots ~~associated with the functional unit~~.

38. (currently amended) The processor-readable medium of claim 36, further containing processor-executable instructions for:

determining a number of input registers and a number of output registers that are used by the first instruction; and

when the first instruction uses at most two input registers and one output register, replacing ~~mapping~~ the first instruction with the second instruction, the second instruction being associated with ~~to~~ a single issue slot.

39-40. (cancelled)

41. (currently amended) The processor-readable medium of claim 36, wherein the second instruction is associated with ~~further containing processor-executable instructions for mapping the instruction to~~ two or more ~~a plurality of~~ issue slots.

42. (currently amended) The processor-readable medium of claim 36, wherein the first instruction is a shuffle operation.

43. (currently amended) The processor-readable medium of claim 36, wherein the first instruction is a floating point operation.

44. (new) A method for compiling a software program for a programmable processor having a functional unit associated with at least two issue slots, the method comprises:

identifying source operations from a set of processor-executable operations that produce operands of a first processor-executable operation;

placing commands for the source operations in one or more instruction words;

selecting an earliest instruction word from a set of instruction words after the one or more instruction words in which commands for the source operations have already been placed;

determining whether the first processor-executable operation can be replaced by a second equivalent processor-executable operation;

replacing the first processor-executable operation with the second equivalent processor-executable operation if it is determined that the first processor-executable operation can be so replaced;

determining whether an instruction word can be constructed that contains the commands already included in the earliest instruction word and commands for the first processor-executable operation or the second processor-executable operation if it has replaced the first processor-executable operation; and

if such an instruction word can be constructed, updating the earliest instruction word to include the commands for the first processor-executable operation or the second processor-executable operation if it has replaced the second processor-executable operation.

45. (new) The method of claim 44, further comprising:

if such an instruction word cannot be constructed, selecting an subsequent instruction word after the earliest instruction word; and

determining whether an instruction word can be constructed that contains the commands already included in the subsequent instruction word and commands for the

first processor-executable operation or the second processor-executable operation if it has replaced the first processor-executable operation.

46. (new) A processor-readable medium having processor-executable instructions for:

identifying source operations from a set of processor-executable operations that produce operands of a first processor-executable operation;

placing commands for the source operations in one or more instruction words;

selecting an earliest instruction word from a set of instruction words after the one or more instruction words in which commands for the source operations have already been placed;

determining whether the first processor-executable operation can be replaced by a second equivalent processor-executable operation;

replacing the first processor-executable operation with the second equivalent processor-executable operation if it is determined that the first processor-executable operation can be so replaced;

determining whether an instruction word can be constructed that contains the commands already included in the earliest instruction word and commands for the first processor-executable operation or the second processor-executable operation if it has replaced the first processor-executable operation; and

if such an instruction word can be constructed, updating the earliest instruction word to include the commands for the first processor-executable operation or the second processor-executable operation if it has replaced the second processor-executable operation.

47. (new) The processor-readable medium of claim 46, having further processor-executable instructions for:

if such an instruction word cannot be constructed, selecting an subsequent instruction word after the earliest instruction word,; and

determining whether an instruction word can be constructed that contains the commands already included in the subsequent instruction word and commands for the first processor-executable operation or the second processor-executable operation if it has replaced the first processor-executable operation.